REMARKS

Claims 1-20 remain in the present application. Applicants respectfully request further examination and reconsideration of the rejections based on the above amendments and the arguments set forth below.

35 U.S.C. Section 112 rejections

Claims 1-20 are rejected under 35 U.S.C. Section 112 as being indefinite. Applicants respectfully traverse.

Paragraph 3 of the above referenced Office Action rejects Claim 1 under 35 U.S.C. Section 112, regarding the definiteness of the limitation "a virtual microcontroller having means for detecting a sequence of instructions, for computing a conditional jump address, and for determining after receipt of the I/O read data from the microcontroller whether to proceed with instruction execution." Applicants refer to page 9 of the present specification, lines 16-25, and point out one description of the elements comprising a virtual microcontroller as in the claimed invention. One embodiment of the virtual microcontroller is described as being based on a general-purpose programmable hardware device (base station 218), such as a gate array, and is configured to function as a functionally equivalent device-under-test, in this case a microcontroller. The base station is configured as an emulator of the internal microprocessor portion of a microcontroller. A field

programmable gate array (FPGA), or other programmable logic device, can be configured to function as the virtual microcontroller.

Thus, the internal microprocessor portion of the microcontroller, as implemented by a programmable logic device, executes computer readable code, decodes instructions, increments program counters, computes addresses, and the like, in the manner of a real microcontroller. Accordingly, Applicants assert that what is meant by the term "virtual microcontroller" as used in the present specification is definite to one skilled in the art. Furthermore, Applicants assert that the claim limitations regarding detecting an I/O read instruction followed by a conditional jump instruction are definite to one skilled in the art. The mechanisms by which a programmable device, such as a microprocessor or microcontroller, recognizes instructions is understood by those skilled in the art.

With regard to the description of steps performed by the virtual microcontroller which are described "in narrative" by the specification of the present application, Applicants point out that such descriptions of steps performed by a programmable device are common and well understood by those skilled in the art. For example, the implementation of one or more functions of a programmable device (e.g., microprocessor, microcontroller, etc.) can be purely hardware based (e.g., combinational logic), software based (e.g., sequential logic), or some combination of the two. In each instance, the

functionality is definite and is understood to be so by one skilled in the art, irrespective of the fact that the function may be narratively described as the programmable device performing the function (e.g., the programmable device executing, reading, communicating, jumping, etc.). Applicants assert that this same characteristic is true for a virtual microcontroller as defined by the present specification. For example, using the configurable logic and memory of an FPGA, one or more functions can be implemented such that they are hardware based, software based, or based upon some combination of the two, and descriptions of such functions may be narrative in nature.

With regard to the decoding and execution of instructions, as disclosed on page 26 at lines 17 through 29 of the present specification, Applicants point out that one skilled in the art would understand that the detecting and executing of instructions by a microcontroller or a virtual microcontroller is with regard to machine readable instructions, and the description of such instructions using assembly code, as at page 26 lines 17 through 29, is for the benefit of the reader.

With regard to the "means for" limitations, Applicants have herein amended the recited means to more particularly point out that the virtual microcontroller has means for detecting an I/O read instruction followed by a conditional jump instruction. For the rational described above, Applicants assert that this limitation is definite to one skilled in the art. Furthermore,

the independent claims have been amended to particularly point out that the specific instructions that are detected are an I/O read instruction followed by an I/O write instruction. Applicants assert that the meaning of such limitations as described by the specification of the present application and as recited by the claims is definite to one skilled in the art.

Accordingly, Applicants respectfully submit that in view of the above amendments, all claims of the present application are definite within the meaning of 35 U.S.C. Section 112.

35 U.S.C. Section 103 rejections

Paragraph 13 of the above referenced Office Action rejects independent Claims 1, 6, and 14 under 35 U.S.C. Section 103 as being unpatentable over Profit (U.S. Patent No. 5,911,059) in view of Barnett (U.S. Patent No. 6,173,419). Applicants respectfully traverse.

Embodiments of the claimed invention as recited in independent Claims 1, 6, and 14, include an In-Circuit Emulation (ICE) system utilizing a real microcontroller operating in lock-step with a virtual microcontroller. The real microcontroller and the virtual microcontroller operate in lockstep so that registers, memory locations and other debugged data can be retrieved from the virtual microcontroller without disrupting operation of a real microcontroller. When an I/O read instruction is carried out followed by a

conditional jump instruction dependent upon the I/O read data (e.g., a branch instruction), the virtual microcontroller, executing in lockstep with the real microcontroller, does not have adequate time to compute the jump address after receipt of I/O read data from the real microcontroller. As recited in each of the independent claims, the virtual microcontroller receives the I/O data from the real microcontroller (e.g., as opposed to implementing its own I/O). Accordingly, the virtual microcontroller cannot compute the jump address in sufficient time to remain in lockstep execution with the real microcontroller. Thus, when this sequence of instructions is detected, the virtual microcontroller pre-calculates the jump address and makes the jump decision after receipt of the I/O read data from the real microcontroller.

Applicants point out that the cited Profit-Barnett combination does not disclose or suggest a virtual microcontroller coupled to and executing instructions in lock-step with a real microcontroller, wherein the microcontroller sends I/O read data to the virtual microcontroller, as opposed to the virtual microcontroller implementing its own I/O. Applicants point out that the cited combination does not disclose or suggest the virtual microcontroller detecting an I/O read instruction followed by a conditional jump instruction, and the virtual microcontroller computing a conditional jump address prior to receipt of I/O read data from the microcontroller.

Furthermore, Applicants point out that the cited combination does not disclose any motivation or any discussion as to the reasoning behind why the computing of a conditional jump address prior to receipt of I/O read data from the microcontroller would be preferable. Applicants find no disclosure regarding the problems of maintaining lockstep execution while also implementing I/O between an ICE unit and a real device under test. There is no discussion of how such features can be implemented without altering the program code of the real device under test (e.g., by inserting wait states or the like).

Accordingly, Applicants assert that the present invention as recited in Claims 1-20 is not rendered obvious by the cited combination within the meaning of 35 U.S.C. Section 103.

CONCLUSION

Applicants respectfully assert that all claims (Claims 1-20) are in condition for allowance and Applicants earnestly solicit such action from the Examiner.

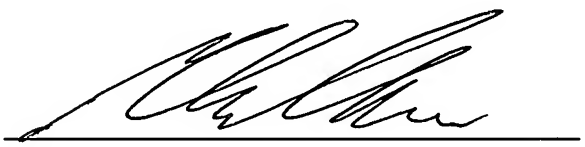
The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO, LLP

Dated: 8/17, 2005



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